FIG.1

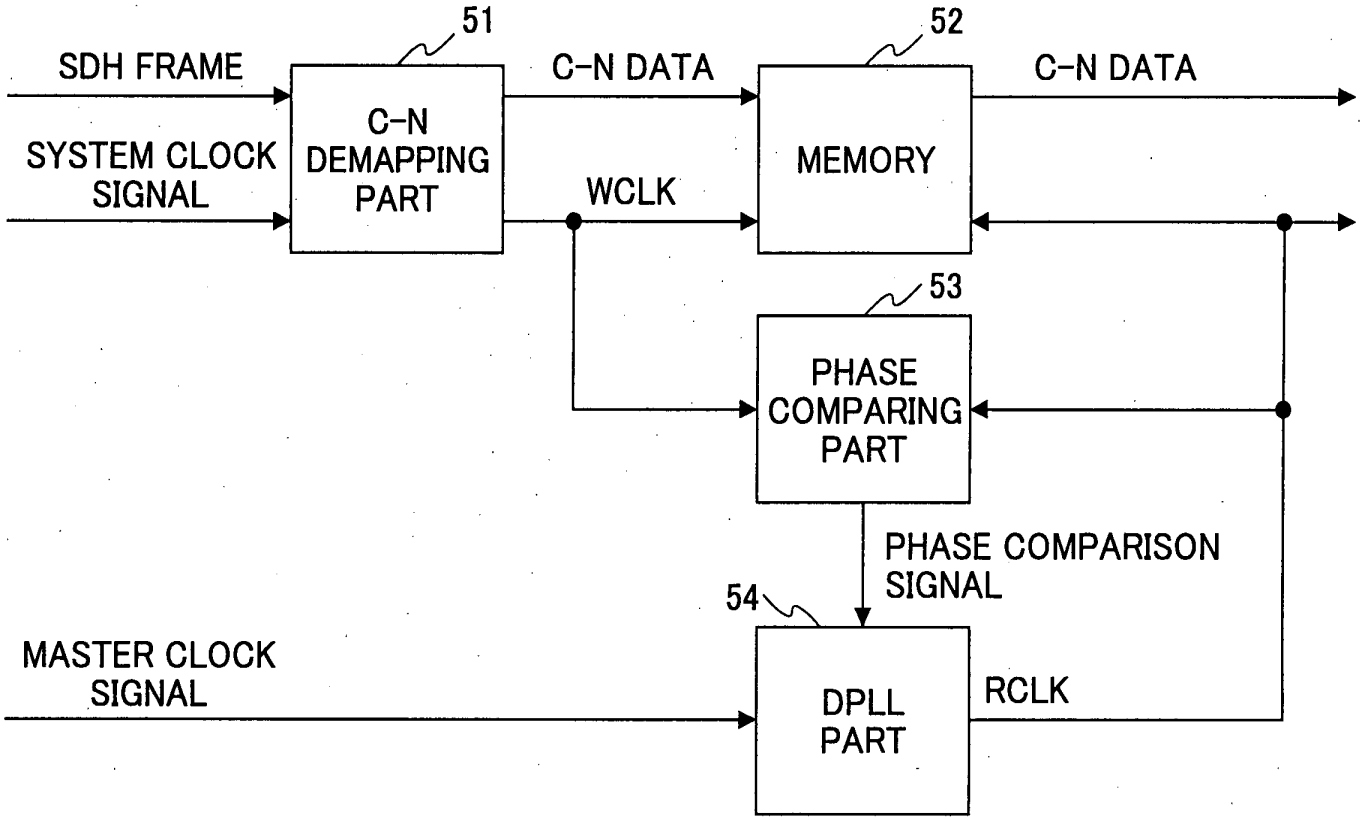
51
52
SDH FRAME
C-N DATA
C-N DATA
C-N DEMAPPING PART
SYSTEM CLOCK SIGNAL
WCLK
MEMORY
53
PHASE COMPARING PART
PHASE COMPARISON SIGNAL
54
MASTER CLOCK SIGNAL
DPLL PART
RCLK

FIG.2

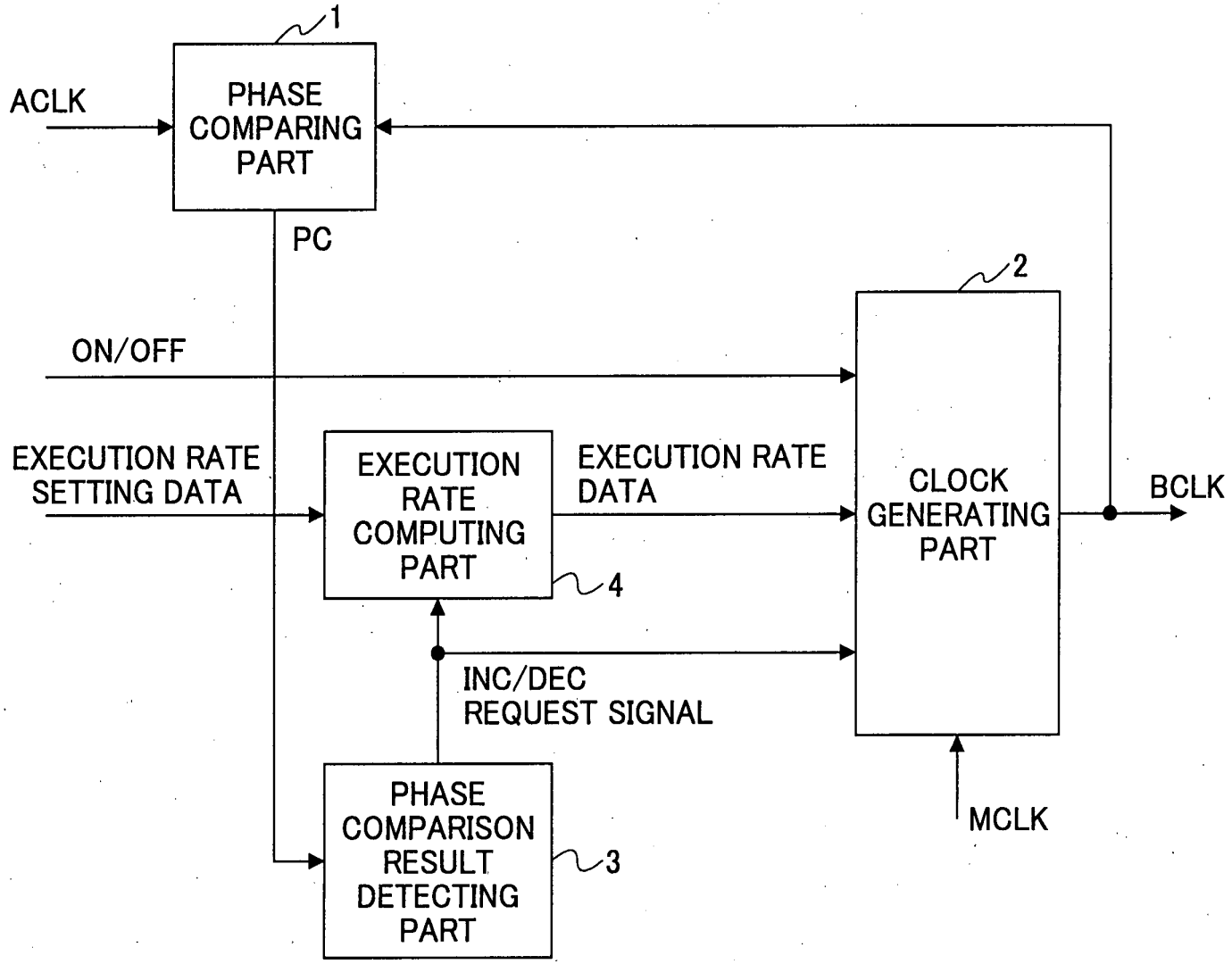
1
ACLK
PHASE COMPARING PART
PC
2
ON/OFF
EXECUTION RATE SETTING DATA
EXECUTION RATE COMPUTING PART
4
EXECUTION RATE DATA
CLOCK GENERATING PART
BCLK
INC/DEC REQUEST SIGNAL
MCLK
PHASE COMPARISON RESULT DETECTING PART
3

FIG.3

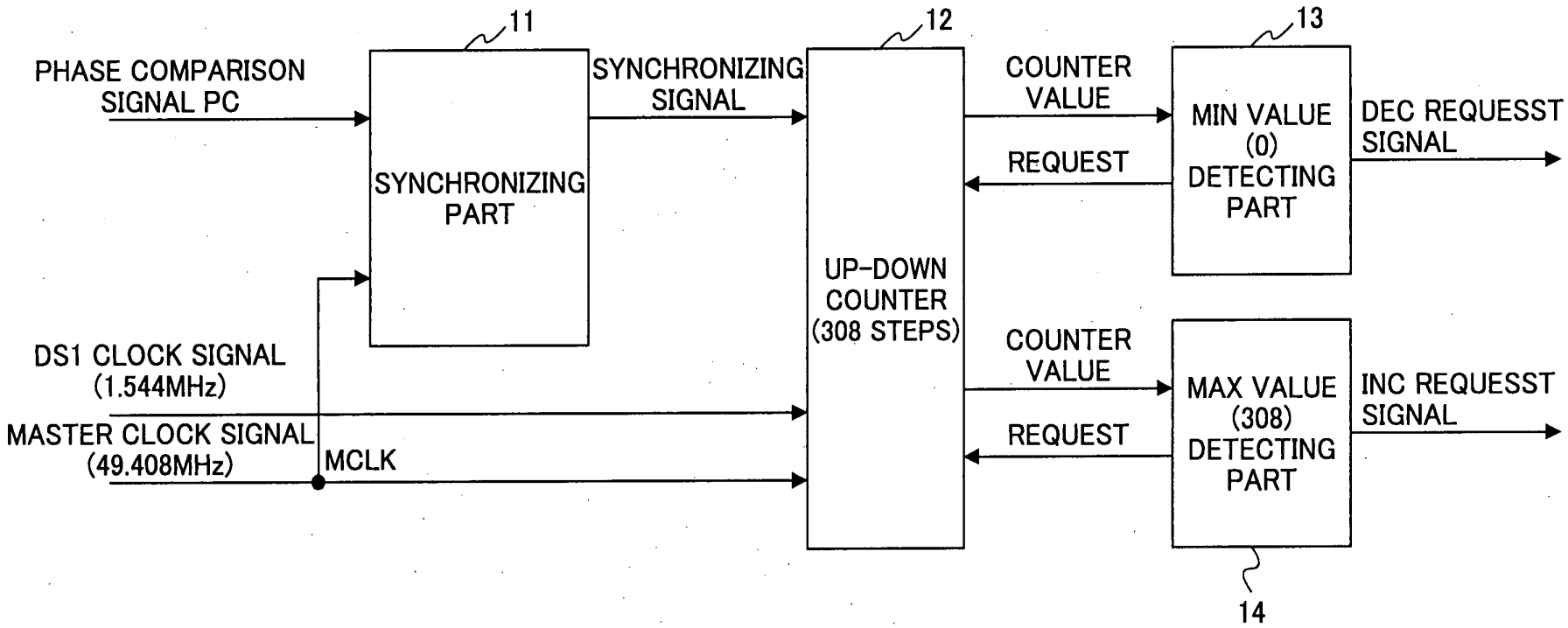
11
12
13
PHASE COMPARISON SIGNAL PC
SYNCHRONIZING PART
SYNCHRONIZING SIGNAL
UP-DOWN COUNTER (308 STEPS)
COUNTER VALUE
REQUEST
MIN VALUE (0) DETECTING PART
DEC REQUESST SIGNAL
DS1 CLOCK SIGNAL (1.544MHz)
MASTER CLOCK SIGNAL (49.408MHz)
MCLK
COUNTER VALUE
REQUEST
MAX VALUE (308) DETECTING PART
INC REQUESST SIGNAL
14

FIG.4A

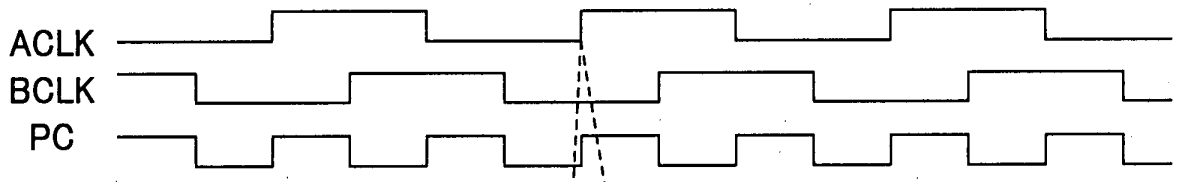

FIG.4B

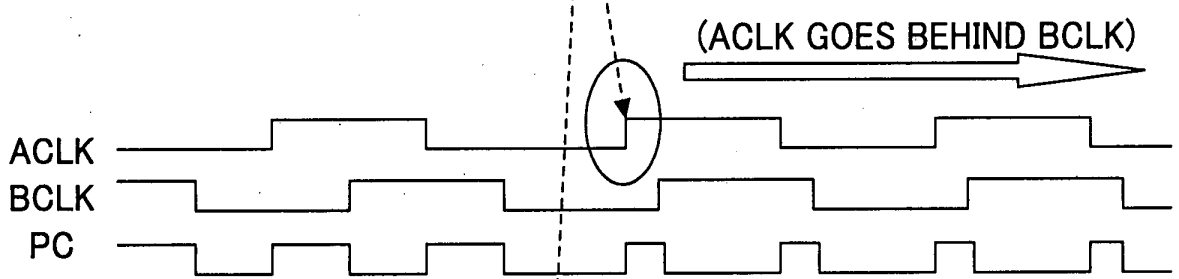

FIG.4C

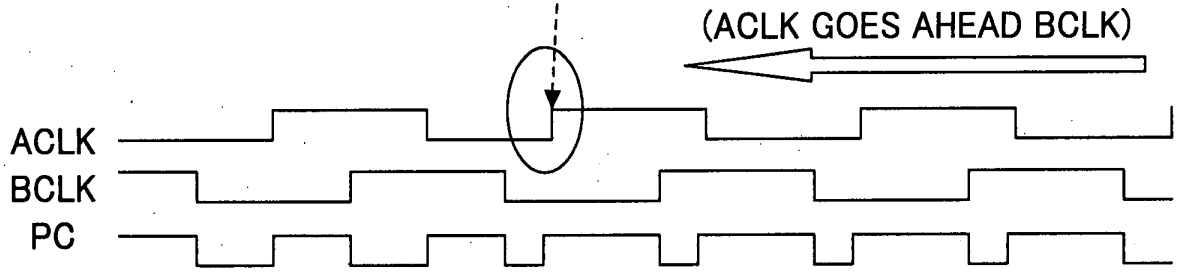

FIG.5A

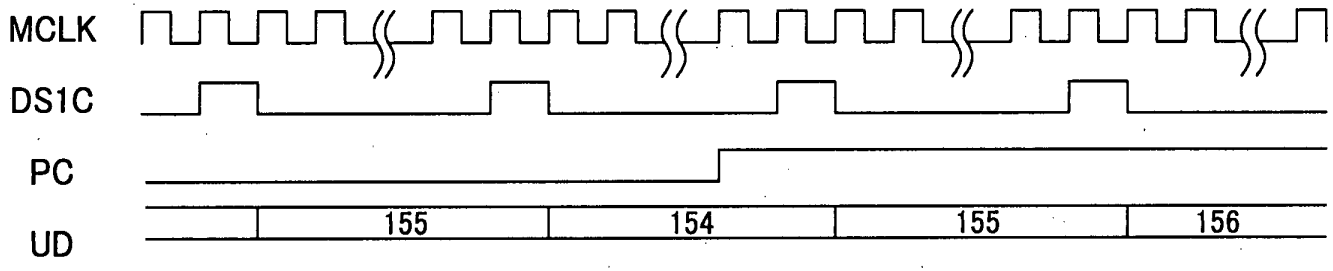

FIG.5B

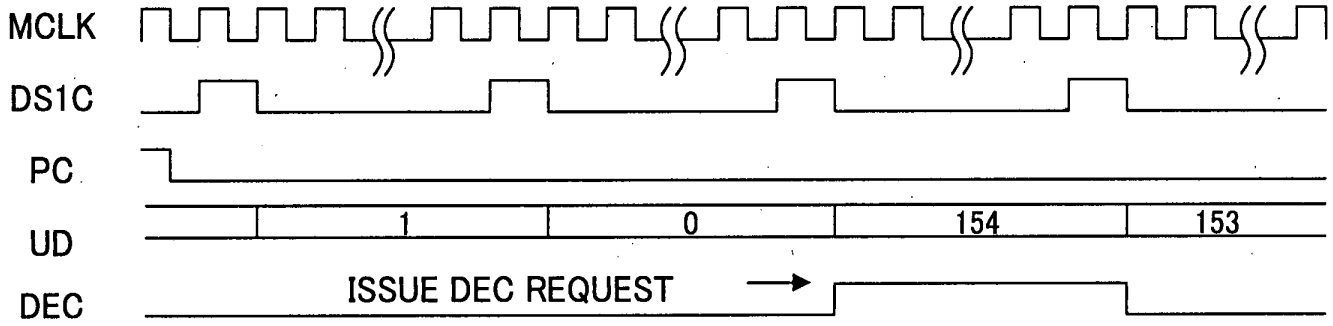

FIG.5C

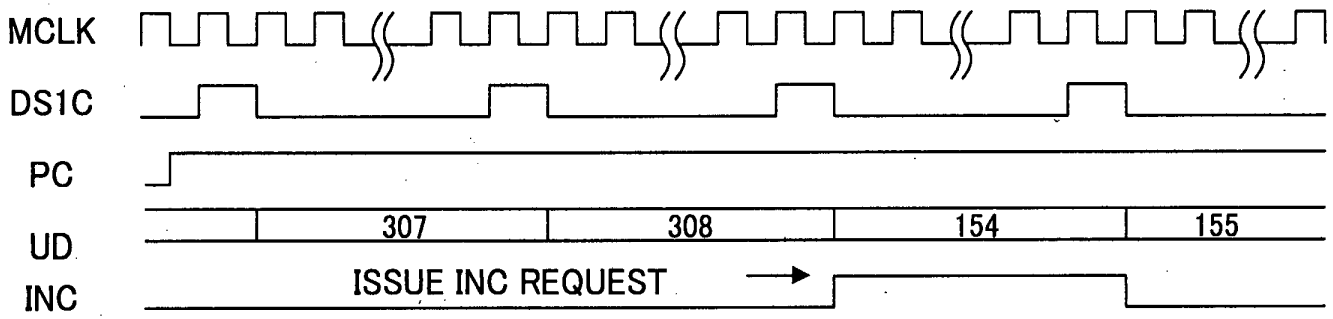

FIG.6

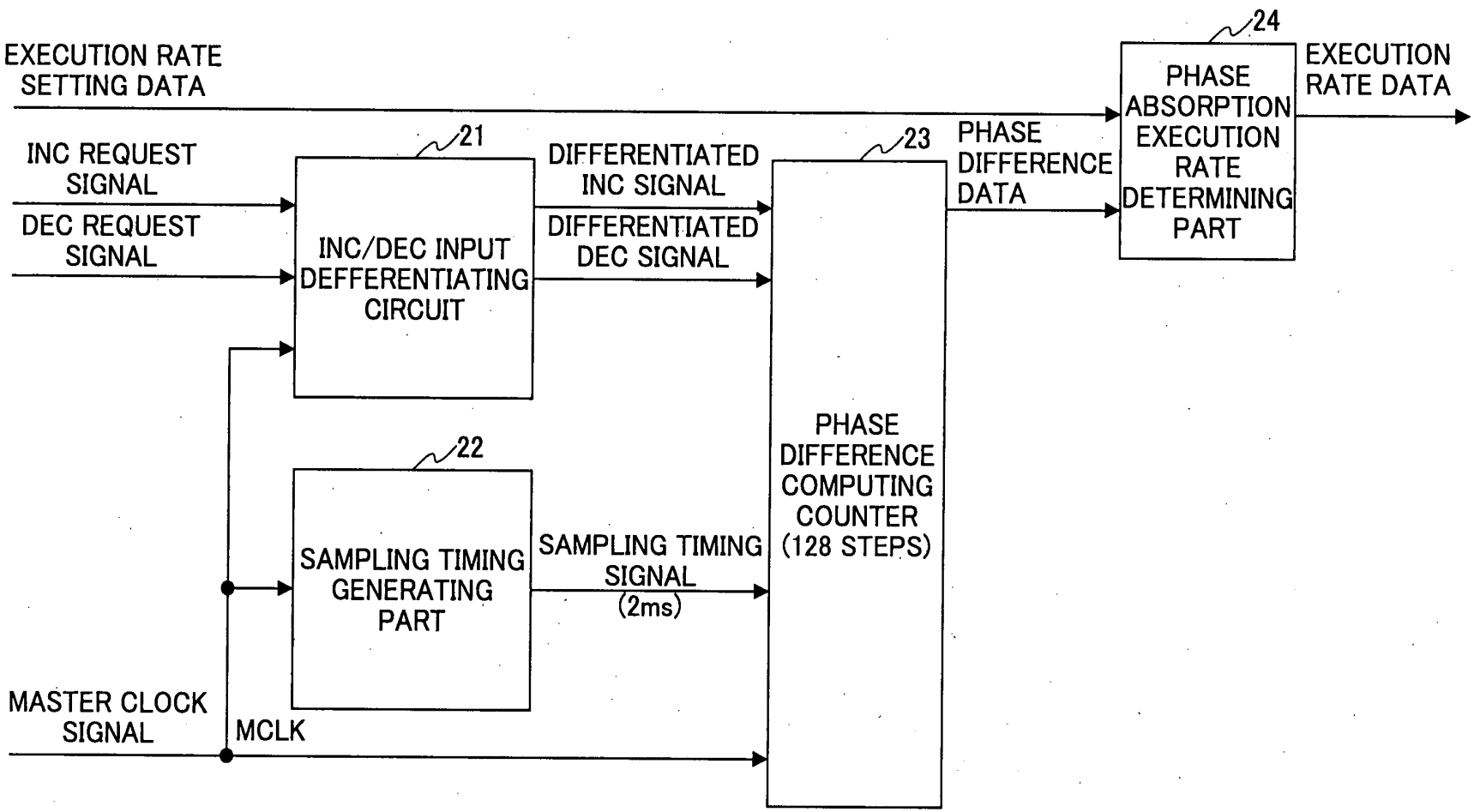
EXECUTION RATE SETTING DATA
INC REQUEST SIGNAL
DEC REQUEST SIGNAL
21
INC/DEC INPUT DEFFERENTIATING CIRCUIT
DIFFERENTIATED INC SIGNAL
DIFFERENTIATED DEC SIGNAL
23
PHASE DIFFERENCE COMPUTING COUNTER (128 STEPS)
PHASE DIFFERENCE DATA
24
PHASE ABSORPTION EXECUTION RATE DETERMINING PART
EXECUTION RATE DATA
22
SAMPLING TIMING GENERATING PART
SAMPLING TIMING SIGNAL (2ms)
MASTER CLOCK SIGNAL
MCLK

FIG.7

PHASE DIFFERENCE	EXECUTION RATE	PHASE DIFFERENCE	EXECUTION RATE	PHASE DIFFERENCE	EXECUTION RATE	PHASE DIFFERENCE	EXECUTION RATE	PHASE DIFFERENCE	EXECUTION RATE
50bit	1/1	40bit	1/1	30bit	3/4	20bit	1/2	10bit	1/2
49bit	1/1	39bit	1/1	29bit	3/4	19bit	1/2	9bit	1/2
48bit	1/1	38bit	1/1	28bit	3/4	18bit	1/2	8bit	1/2
47bit	1/1	37bit	1/1	27bit	3/4	17bit	1/2	7bit	1/2
46bit	1/1	36bit	1/1	26bit	1/2	16bit	1/2	6bit	1/4
45bit	1/1	35bit	3/4	25bit	1/2	15bit	1/2	5bit	1/2
44bit	1/1	34bit	3/4	24bit	1/2	14bit	1/2	4bit	1/2
43bit	1/1	33bit	3/4	23bit	1/2	13bit	3/4	3bit	1/2
42bit	1/1	32bit	3/4	22bit	1/2	12bit	3/4	2bit	1/2
41bit	1/1	31bit	3/4	21bit	1/2	11bit	3/4	1bit	1/2

FIG.8A

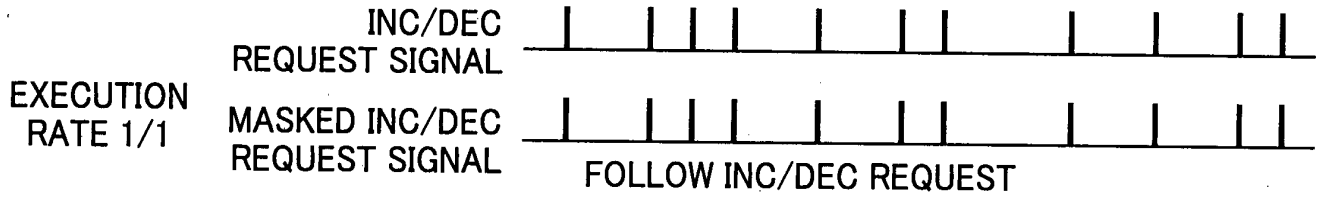

FIG.8B

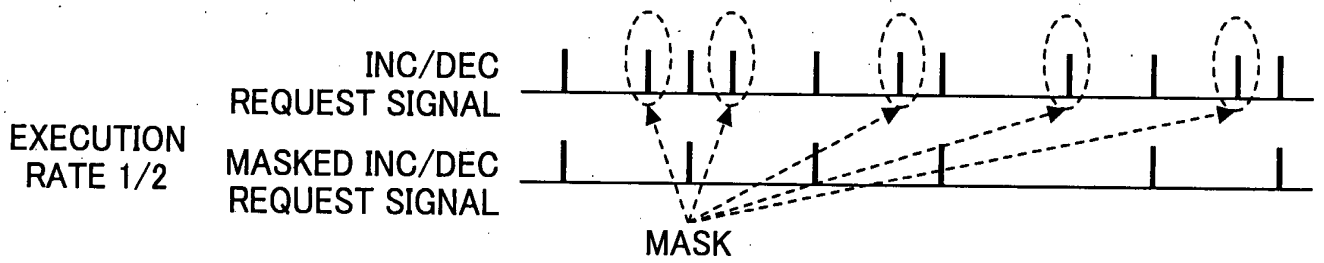

FIG.8C

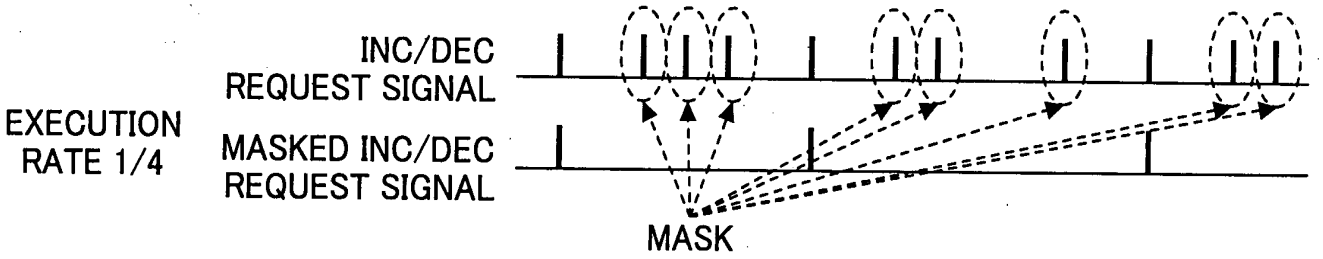

FIG.8D

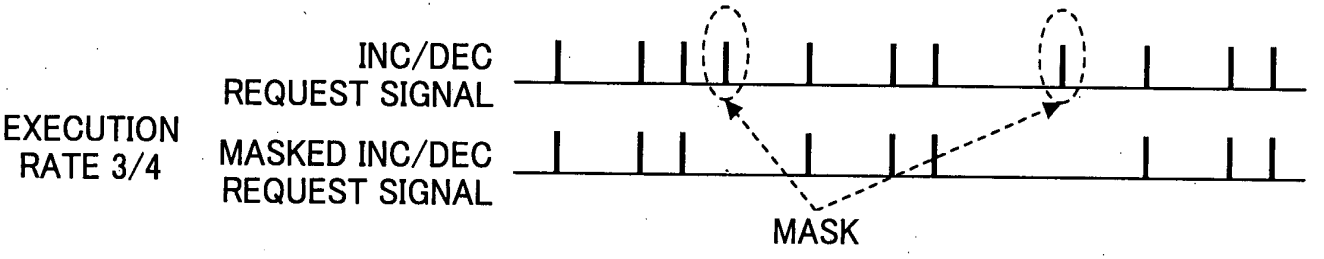

FIG.9

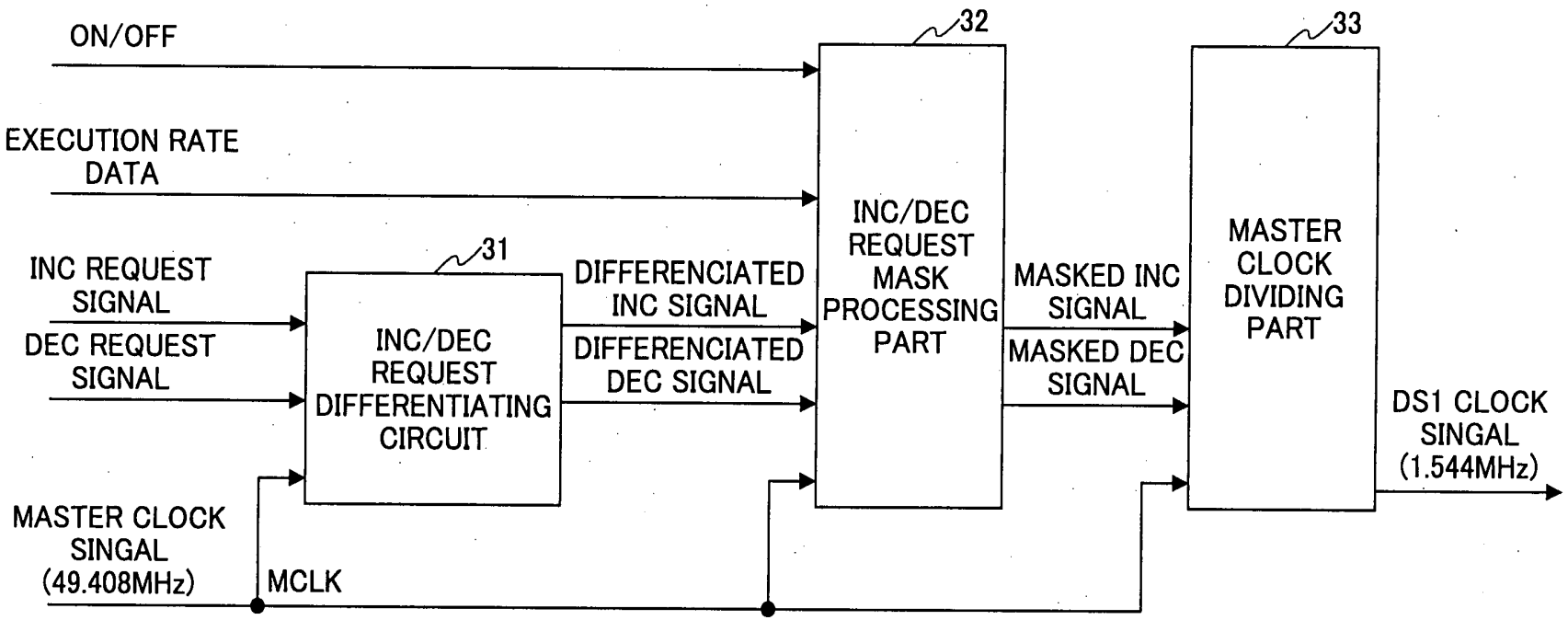
ON/OFF
EXECUTION RATE DATA
INC REQUEST SIGNAL
DEC REQUEST SIGNAL
31
INC/DEC REQUEST DIFFERENTIATING CIRCUIT
DIFFERENCIATED INC SIGNAL
DIFFERENCIATED DEC SIGNAL
32
INC/DEC REQUEST MASK PROCESSING PART
MASKED INC SIGNAL
MASKED DEC SIGNAL
33
MASTER CLOCK DIVIDING PART
DS1 CLOCK SINGAL (1.544MHz)
MASTER CLOCK SINGAL (49.408MHz)
MCLK

FIG.10A

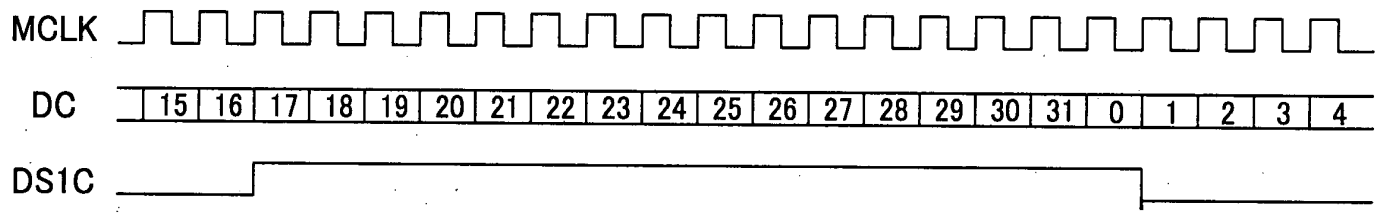

FIG.10B

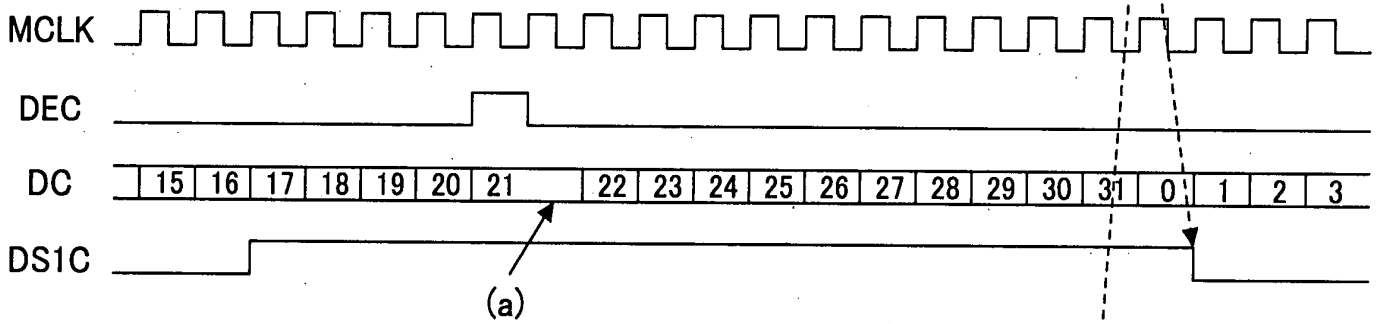

FIG.10C

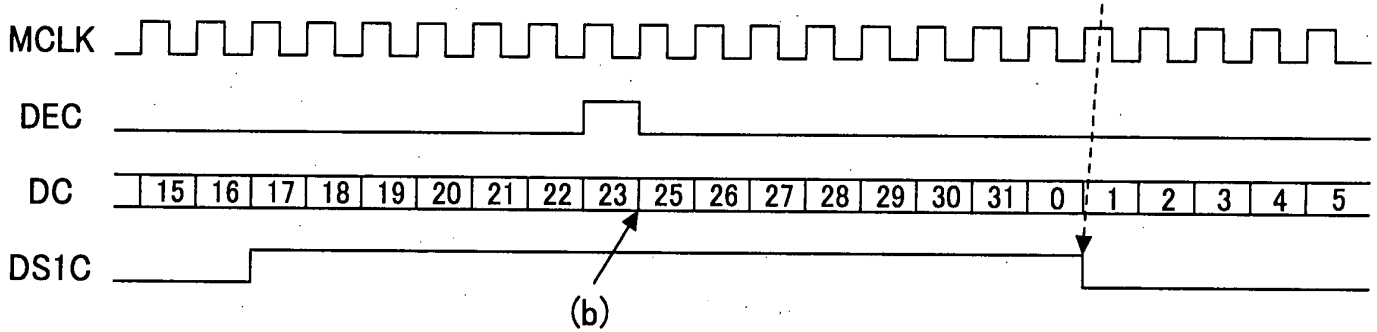

FIG.11A

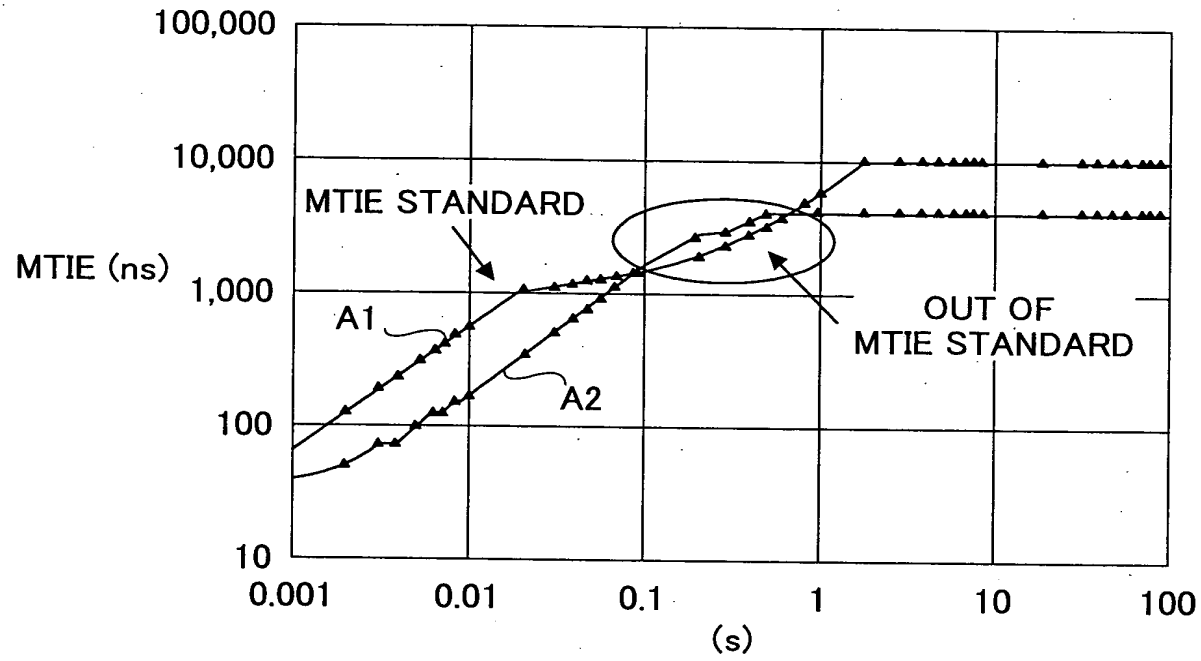
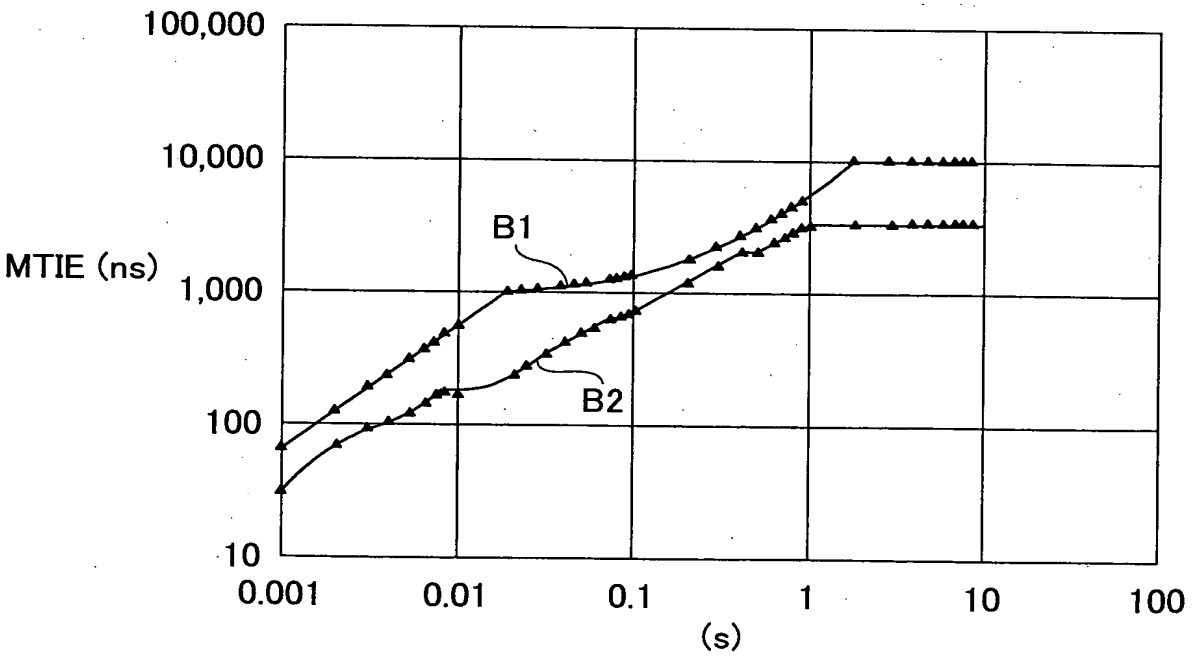
FIG.11B